Power MOSFET

24 V, 110 A, N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low R_{DS(on)} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High–Efficiency DC–DC Converters
- Pb-Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	24	V	
Gate-to-Source Voltage - Continuous	V_{GS}	±20	V	
Thermal Resistance – Junction–to–Case	$R_{\theta JC}$	1.35	°C/W	
Total Power Dissipation @ T _C = 25°C	P _D	110	W	
Drain Current - Continuous @ T _C = 25°C, Chip	I _D	110	Α	
- Continuous @ $T_C = 25$ °C, Chip		110	Â	
Limited by Package	I _D	110	_ ^	
- Continuous @ T _A = 25°C,	I _D	32	Α	
Limited by Wires				
– Single Pulse (t _p = 10 μs)	I_{D}	110	Α	
Thermal Resistance				
Junction–to–Ambient (Note 1)	$R_{\theta JA}$	52	°C/W	
– Total Power Dissipation @ T_A = 25°C	P_{D}	2.88	W	
– Drain Current – Continuous @ T _A = 25°C	I_{D}	17.5	Α	
Thermal Resistance				
– Junction–to–Ambient (Note 2)	$R_{\theta JA}$	100	°C/W	
Total Power Dissipation @ T_A = 25°C	P_{D}	1.5	W	
– Drain Current – Continuous @ T _A = 25°C	I _D	12.5	Α	
Operating and Storage	T _J , T _{stg}	-55 to	°C	
Temperature Range		175		
Single Pulse Drain-to-Source Avalanche	E _{AS}	120	mJ	
Energy – Starting T _J = 25°C				
$(V_{DD} = 50 \text{ Vdc}, V_{GS} = 10 \text{ Vdc},$				
$I_L = 15.5 \text{ Apk}, L = 1.0 \text{ mH}, R_G = 25 \Omega$				
Maximum Lead Temperature for Soldering	TL	260	°C	
Purposes, (1/8" from case for 10 s)				

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- 1. When surface mounted to an FR4 board using 0.5 sq in drain pad size.
- When surface mounted to an FR4 board using the minimum recommended pad size.

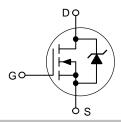


ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX	
24 V	4.1 mΩ @ 10 V	110 A	

N-Channel



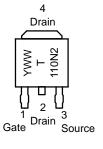


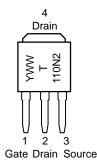
CASE 369AA DPAK (Surface Mount) STYLE 2



CASE 369D DPAK (Straight Lead) STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS





Y = Year WW = Work Week T110N2 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Ch	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS				•	-	•
Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 V, I _D = 250 μA) Positive Temperature Coefficient		V _{(BR)DSS}	24	28 15		V mV/°C
Zero Gate Voltage Drain Curre $(V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V})$ $(V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 0 \text{ V})$	I _{DSS}			1.5 10	μΑ	
Gate-Body Leakage Current (\	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	I _{GSS}			±100	nA
ON CHARACTERISTICS (Note	3)					
Gate Threshold Voltage (Note $(V_{DS} = V_{GS}, I_D = 250 \mu A)$ Negative Threshold Temperatu	V _{GS(th)}	1.0	1.5 5.0	2.0	V mV/°C	
Static Drain-to-Source On-Re ($V_{GS} = 10 \text{ V}, I_D = 110 \text{ A}$) ($V_{GS} = 4.5 \text{ V}, I_D = 55 \text{ A}$) ($V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$) ($V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$)	R _{DS(on)}		4.1 5.5 3.9 5.5	4.6 6.2	mΩ	
Forward Transconductance (V _I	_{DS} = 10 V, I _D = 15 A) (Note 3)	9FS		44		Mhos
DYNAMIC CHARACTERISTICS	1			•	•	•
Input Capacitance		C _{iss}		2710	3440	pF
Output Capacitance	$(V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz})$	C _{oss}		1105	1670	
Transfer Capacitance	,			450	640	1
SWITCHING CHARACTERISTIC	CS (Note 4)					
Turn-On Delay Time		t _{d(on)}		11	22	ns
Rise Time	(V _{GS} = 10 V, V _{DD} = 10 V,	t _r		39	80	
Turn-Off Delay Time	$I_D = 40 \text{ A}, R_G = 3.0 \Omega$	t _{d(off)}		27	40	
Fall Time	1	t _f		21	40	
Gate Charge		Q _T		23.6	28	nC
	$(V_{GS} = 4.5 \text{ V}, I_D = 40 \text{ A}, V_{DS} = 10 \text{ V}) \text{ (Note 3)}$	Q_{GS}		5.1		
	55 - 7 (7	Q _{DS}		11		
SOURCE-DRAIN DIODE CHAR	ACTERISTICS	-		•	-	-
Forward On–Voltage	$(I_S = 20 \text{ A}, V_{GS} = 0 \text{ V}) \text{ (Note 3)}$ $(I_S = 55 \text{ A}, V_{GS} = 0 \text{ V})$ $(I_S = 20 \text{ A}, V_{GS} = 0 \text{ V}, T_J = 125^{\circ}\text{C})$	V _{SD}		0.82 0.99 0.65	1.2	V
Reverse Recovery Time		t _{rr}		36.5		ns
	$(I_S = 30 \text{ A}, V_{GS} = 0 \text{ V},$ $dI_S/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 3)}$	ta		30		
	. 5	t _b		25		
Reverse Recovery Stored Cha	Q_{rr}		0.048		μC	

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

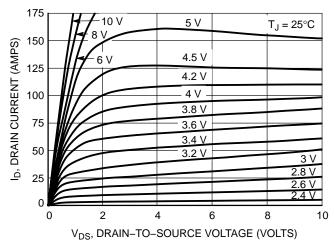
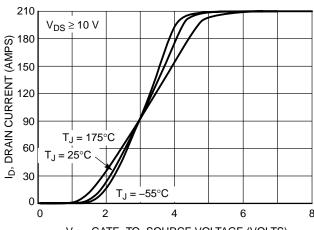


Figure 1. On-Region Characteristics



V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 2. Transfer Characteristics

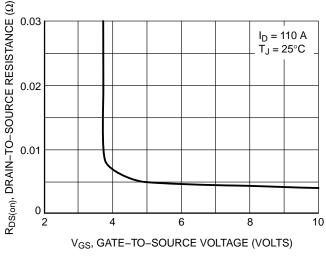


Figure 3. On–Resistance versus Gate–to–Source Voltage

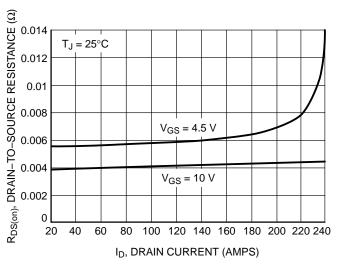


Figure 4. On–Resistance versus Drain Current and Gate Voltage

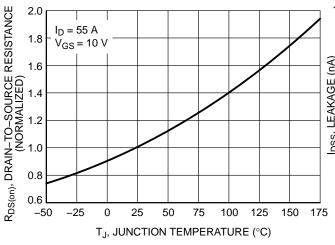


Figure 5. On–Resistance Variation with Temperature

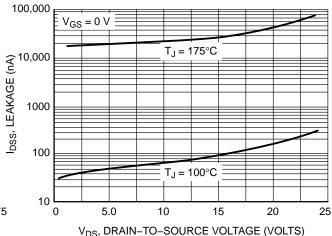
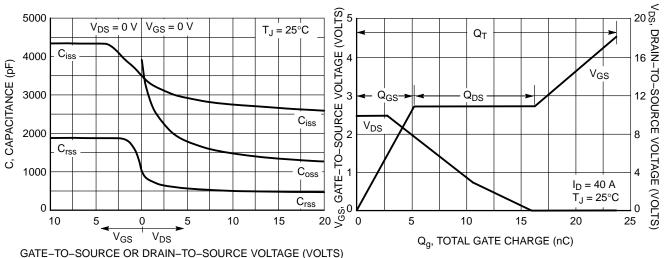


Figure 6. Drain-to-Source Leakage Current versus Voltage



TIE-10-300RCE OR DRAIN-10-300RCE VOLIAGE (VOLIS

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

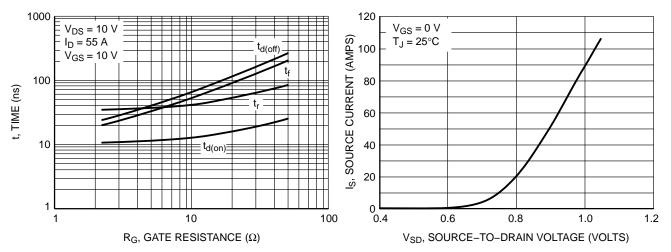


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

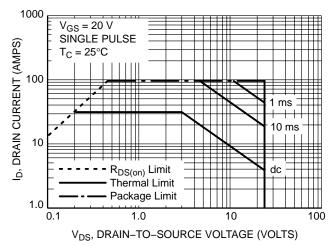


Figure 11. Maximum Rated Forward Biased Safe Operating Area

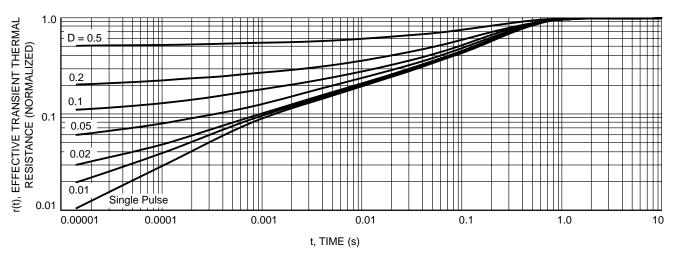


Figure 12. Thermal Response

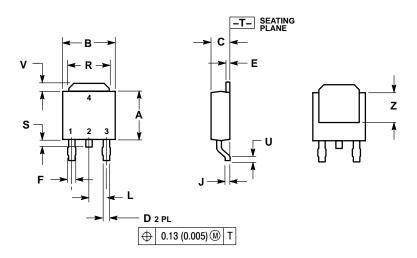
ORDERING INFORMATION

Device	Package	Shipping [†]	
NTD110N02R	DPAK	75 Units/Rail	
NTD110N02RG	DPAK (Pb-Free)	75 Units/Rail	
NTD110N02R-001	DPAK (Straight Lead)	75 Units/Rail	
NTD110N02R-001G	DPAK (Straight Lead) (Pb-Free)	75 Units/Rail	
NTD110N02RT4	DPAK	2500 Tape & Reel	
NTD110N02RT4G	DPAK (Pb-Free)	2500 Tape & Reel	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK CASE 369AA-01 ISSUE O

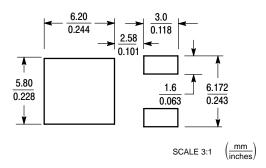


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
Е	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC 2.29 BS0		BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020		0.51	
٧	0.035	0.050	0.89	1.27
z	0.155		3.93	

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

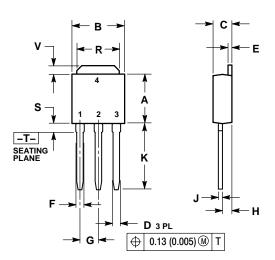
SOLDERING FOOTPRINT*

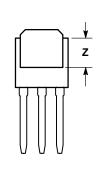


*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK CASE 369D-01 **ISSUE O**





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
Н	0.034	0.040	0.87 1.01	
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2:

PIN 1. GATE

- DRAIN 2.
- 3. SOURCE DRAIN

ON Semiconductor and was are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its partnif rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.